

WHAT IS CLAIMED IS:

1. A programmable metal-oxide-semiconductor (MOS) memory circuit comprising:
 - a data read module having a first output and a second output based on a voltage difference between a first input and a second input;
 - a first polycrystalline resistor having a first end connectable to a first control voltage level, and a second end connected to a second control voltage level;
 - a second polycrystalline resistor having a first end connectable to a first control voltage level, and a second end connected to a second control voltage level; and
 - a connection module for connecting the first ends of the first and second resistors to the first and second inputs respectively,wherein the first and second control voltage levels are imposed to program either the first or second resistor by causing a current stress across the resistor, and wherein the first and second outputs of the data read module produce voltage results representing the programmed value of the first or second resistor when the connection module is enabled.
2. The circuit of claim 1 wherein the first voltage level is imposable through a P-type MOS transistor to the first end of the first or second resistor.
3. The circuit of claim 2 wherein the P-type MOS transistor is a thick oxide MOS transistor.
4. The circuit of claim 1 wherein the first control voltage level is higher than the

operating voltage.

5. The circuit of claim 1 wherein the second control voltage level is at a ground level.
6. The circuit of claim 1 wherein the voltage result represents either a logical one (1) or a logical zero (0).
7. The circuit of claim 1 wherein the first and second outputs of the data read module are complementary to each other.
8. The circuit of claim 1 wherein the connection module has two N-type devices with their gates connected together to a third control voltage level.
9. The circuit of claim 8 wherein the N-type devices are thick oxide MOS devices.
10. A method for programming a metal-oxide-semiconductor (MOS) memory circuit, the circuit comprising a data read module having a first input and a second input and one or more outputs, a first and second polycrystalline resistors having their first ends connectable to a first control voltage level and their second end connected to a second voltage level, and a connection module for connecting the first ends of the first and second resistors to the first and second inputs respectively, the method comprising:
disenabling the connection module for disconnecting the first ends of the resistors from the first and second inputs;

imposing the first control voltage on the first end of the first or second resistor; and

relieving the first control voltage from the connected first end of either the first or second resistor.

11. The method of claim 10 further comprising obtaining one or more voltage results from the outputs of the data read module representing whether the first or second resistor has been programmed.

12. The method of claim 11 wherein the obtaining further includes:
enabling the connection module for connecting the first end of the first resistor to the first input, and the first end of the second resistor to the second input;
and

generating a first voltage result representing that the first or second resistor has been programmed by comparing the voltage difference between the first input and the second input.

13. The method of claim 10 wherein the first control voltage level is imposable through a P-type MOS transistor to cause the current stress across the first or second resistor.

14. The method of claim 10 wherein the first voltage level is higher than an operating voltage of the data read module.

15. The method of claim 10 wherein the second voltage level is at a ground level.

16. A programmable metal-oxide-semiconductor (MOS) memory circuit comprising:
 - a first polycrystalline resistor having a first end connectable to a first control voltage level, and a second end connectable to a second voltage level; and
 - a second polycrystalline resistor having a first end connectable to the first control voltage level, and a second end connectable to the second voltage level,

wherein the first and second control voltage levels are imposed to program either the first or second resistor by causing a current stress across the resistor for programming the memory circuit.
17. The circuit of claim 16 wherein the first control voltage level is 3.3V.
18. The circuit of claim 16 wherein the threshold voltage is 1.2V.
19. The circuit of claim 16 further comprising:
 - a latch module having a first output and a second output based on a voltage difference between a first input and a second input,

wherein the first and second inputs are connectable to first ends of the first and second resistors to generate the first and second outputs of the latch representing a programmed value of the first or second resistor.
20. The circuit of claim 19 further comprising a connection module having two N-type transistors with their gates connected together to a third control voltage for connecting the first end of the first resistor to the first input of the latch, and the first end of the second resistor to the second input of the latch.

21. The circuit of claim 16 further comprising a programming triggering module connecting the first voltage level to the first end of the first or second resistor.
22. The circuit of claim 21 wherein the programming triggering module is a P-type MOS device.
23. A polycrystalline silicon resistor pair used in a programmable memory cell comprising:
 - a first polycrystalline silicon resistor stressable by a predetermined current thereacross; and
 - a second polycrystalline silicon resistor similarly structured as the first polycrystalline silicon resistor stressable by the predetermined current, wherein when only the first resistor is stressed by the predetermined current, a resistance of the first resistor is lowered as compared to the unstressed second resistor, thereby programming the memory cell.
24. The memory cell of claim 23 further comprising means for reading the programmed memory cell.
25. The memory cell of claim 24 wherein the means for reading further includes a first output and a second output based on a voltage difference between a first input and a second input, wherein the first and second inputs are connectable to first ends of the first and second resistors to generate the first and second outputs of the latch representing a programmed value of the memory cell.
26. The memory cell of claim 23 further comprising means for imposing the

predetermined current across the first resistor.

27. The memory cell of claim 23 wherein the first and second resistors do not have salicide metal associated therewith.